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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,535	07/17/2003	Martin Blocker	M&N-IT-467	2491
24131	7590	11/03/2005	EXAMINER	
LERNER AND GREENBERG, PA P O BOX 2480 HOLLYWOOD, FL 33022-2480			ROSASCO, STEPHEN D	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/621,535

Applicant(s)

BLOCKER ET AL.

Examiner

Stephen Rosasco

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
4a) Of the above claim(s) 10 and 11 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-9 and 12 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 17 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3/19/04.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

Detailed Action

Applicant's election without traverse of Group I in the reply filed on 9/23/05 is acknowledged. In response to applicant's discussion the examiner will include claim 12 into Group I (claims 1-9 and 12).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu (6,684,382) or Pierrat et al. (6,584,609).

Liu teaches a method for performing optical proximity correction (OPC) of a layout for a layer of material in an integrated circuit (IC) for optical and etch effects, the method comprising: modifying the layout using a first correction process for etch effects; and modifying the layout using a second correction process for optical effects, the second correction using the layout generated by the first correction process as ideal shape for corrections, wherein the first correction process comprises a rule based correction and the second correction process comprises a model based correction process.

And wherein the layout comprised of a plurality of edges, the plurality of edges forming a plurality of features, and wherein the modifying the layout using a first

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correction process further comprises applying the first correction process only to edges having a feature separation over a predetermined amount, n , from edges of other features in the layout.

And wherein etch effects comprise micro loading effects from variable etch rates due to different densities and sizes for features in the layout.

Liu also teaches [006] that microloading refers to the dependence of the etch rate on feature separation for identically sized features and it results from the depletion of reactants when the wafer has a local, higher-density area.

Pierrat et al. teach a method of preparing a semiconductor mask, said method comprising: accepting a semiconductor design;

processing each feature to determine if a ruled-based optical proximity correction system, if a model-based optical proximity correction system, if both rule-based and model-based optical proximity correction systems, or if no correction system should be used for a particular feature, wherein at least one feature comprises a shape;

determining an optimal model from a set of models for correcting each feature to be corrected with said model-based optical proximity correction system;

selectively correcting each feature with a selected correction system determined in said step of processing; and outputting a final corrected semiconductor design.

And wherein the model-based optical proximity correction system handles two or more mask fabrication effects, optical effects, resist processing effects, and etching effects.

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And wherein said features to be corrected with said model-based optical proximity correction system are pre-biased before correcting with said model-based optical proximity correction system.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (6,684,382) or Pierrat et al. (6,584,609) in view of Hoffman et al. (5,552,996)

The claimed invention is directed to a method for correcting local loading effects in the etching of photomasks. The method includes determining a location-dependent density of mask structures resulting in a structure density; determining a location-dependent strength of a loading effect with an aid of the structure density; and determining location-dependent correction values for the mask structures using the location-dependent strength of the loading effect for compensating for the loading effect.

The invention is based on the recognition that the strength of location-dependent loading effects can be predicted with the aid of the location-dependent structure density, and the effects can be compensated.

The applicant discusses the limitations of the prior art in that processing effects in photolithographic mask fabrication can lead to local CD fluctuations. Such processing effects include fogging in electron beam writers, loading in dry etching, or radial effects in connection with spin processing during developing or wet etching.

And that, such effects can be eliminated by processing improvements such as changing the etch chemistry in order to reduce loading effects. But that is expensive and leads to high costs in the mask and/or chip fabrication.

The teachings of Liu or Pierrat et al. differ from those of the applicant in that the applicant teaches that the method comprises determining the location-dependent strength of the loading effect by a convolution of the density function with a Gauss function.

Hoffman et al. teach (see col. 6, line 19+) a method, for controlling a fabrication level of a fabrication process to produce an integrated circuit ("IC") chip, said fabrication level proceeding according to a design pattern, said method comprising the steps of:

(b) automatically establishing a pattern density value for each section of said plurality of sections based upon said portion of said design pattern contained therein; and

(c) controlling said fabrication level based upon said pattern density values established in said step (b) to improve said fabrication process.

And wherein said IC chip fabrication level comprises photo lithographically controlled etching, and wherein said method further comprises, prior to said controlling step (c), automatically adjusting said design pattern as a function of said pattern density values established in said step (b) such that etching errors due to pattern density based etch rate variations are automatically reduced.

And wherein said method further includes automatically establishing, for each section of said plurality of sections of the grid, a first density range as a function of the density value for that section of the grid, said automatically adjusting of said design pattern further comprising automatically adjusting said design pattern as a function of said first density ranges.

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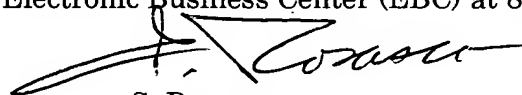
And wherein said design pattern defines a plurality of circuit structures of said IC chip, said method further including assigning a second density range to each circuit structure as a function of said first density ranges of said plurality of sections of said grid, said second density ranges of said circuit structures facilitating said step of automatically adjusting said design pattern to reduce said pattern density based etch rate variations.

Therefore, it would have been obvious to one having ordinary skill in the art to take the teachings of Liu or Pierrat et al. and combine them with the teachings of Hoffman et al. in order to make the claimed invention because the use of the Gaussian distribution function is well known in the art, as well as its combination with other function in order to treat a system which can be modeled with a statistical variation that is considered Gaussian.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



S. Rosasco
Primary Examiner
Art Unit 1756

S. Rosasco
10/31/05